CS-99-120

12GP-2812

November 29, 1999

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 09/418,029 10/14/99

Lap Chan, Cha Cher Liang Randall, Kheng Chok Tee

A NEW METHOD TO FORM A CROSS NETWORK OF AIR GAPS WITHIN IMD LAYER

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,828,121 to Lur et al., "Multi-Level Conduction Structure for VLSI Circuits", describes an air gap between metal lines at different levels by etching the dielectric layers between the metal line levels.

U.S. Patent 5,783,864 to Dawson et al., "Multilevel Interconnect Structure of an Integrated Circuit having Air Gaps and Pillars Separating Levels of Interconnect", describes air gaps and pillars between metal layers.

U.S. Patent 5,561,085 to Gorowitz et al., "Structure of Protecting Air Bridges on Semiconductor Chips from Damage", describes a method for forming air gap bridges.

The following two U.S. Patents describe air gap processes:

1) U.S. Patent 5,461,003 to Havemann et al., "Multilevel Interconnect Structure with Air Gaps Formed Between Metal Leads".
2) U.S. Patent 5,527,737 to Jeng, "Selective Formation of Low-Density, Low-Dielectric-Constant Insulators in Narrow Gaps for Line-To-Line Capacitance Reduction".

U.S. Patent 5,908,318 to Wang et al., "Method of Forming Low Capacitance Interconnect Structures on Semiconducor Substrates", describes an air gap in an ILD by etch out.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37661